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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Frisina, et al.
Serial No: 09/925,080
Filed: August 8, 2001
For: METHOD OF MANUFACTURING AN INTEGRATED EDGE
STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES,
AND RELATED INTEGRATED EDGE STRUCTURE
Confirmation No.: 3073
Examiner: Luu, Chuong A.
Art Unit: 2825

4/13 Amdt
4-2303
Amdt

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on April 16, 2003.

[Signature]
Signature

Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Sir:

In response to the Office Action mailed January 16, 2003, please amend the above-identified application as follows:

IN THE WRITTEN DESCRIPTION

Please rewrite the paragraph beginning on page 1, line 21 to read as follows:

A depletion region is associated with the PN junction, which can be considered as made up of two regions, a first one along the plane portion of the junction, a second one at the edges of said plane portion. The electric field has a different behavior in the two regions. In the plane portion the equipotential lines are parallel to the junction, the maximum electric field is located at the junction and the breakdown occurs when it reaches the critical value E_{CR} . At the junction edges, because of the finite junction depth, the equipotential lines are curved, and spaced closer together than in the plane portion. As a consequence, the electric field increases, and higher electric fields are associated with smaller curvature radii, i.e. a shallower junction. The breakdown voltage of the edge portion of the PN diffused junction is usually lower than that of

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